Bachelor of Technology (Electronics and Communication Engg.)
Scheme of Courses/Examination
(6^{th} SEMESTER)

Sl. No.	Course No.	Subject	Teaching Schedule				Examination Schedule (Marks)				Duration of Exam (Hours)
			L	T	P/D	Tot	Th	Sess	P/VV	Tot	
1	HUT-302E	Fundamentals of Management	3	1	-	4	100	50	-	150	3
2	ECE-302E	Control System Engineering	4	1	-	5	100	50	-	150	3
3	ECE-304E	VHDL & Digital Design	3	1	-	4	100	50	-	150	3
4	ECE-306E	Digital Signal Processing	3	2	-	5	100	50	-	150	3
5	ECE-308E	Digital Communication	3	1	-	4	100	50	-	150	3
6	ECE-310E	Computer Communication Networks	3	1	-	4	100	50	-	150	3
7	ECE-312E	Digital Communication (Pr)	-	-	3	3	-	50	25	75	3
8	ECE-314E	Electronic Design (Pr)	-	-	3	3	-	50	25	75	3
9	ECE-316E	VHDL (Pr)	-	-	3	3	-	50	50	100	3
Total			19	7	9	35	600	450	100	1150	

NOTE: Students will undergo a practical training of 6 weeks duration after the 6^{th} Semester exam

B.TECH VI SEMESTER
CONTROL SYSTEM ENGINEERING
(ECE-302E)

L T P
4 1 -

Theory : 100
Sessional : 50
Time : 3Hrs

UNIT-I :
INTRODUCTION: The control system-open loop & closed loop, servomechanism, stepper motor.
MATHEMATICAL MODELS OF PHYSICAL SYSTEMS: Differential equation of physical systems, transfer function, block diagram algebra, signal flow-graphs , Mason's formula & its application.
FEEDBACK CHARACTERISTICS OF CONTROL SYSTEMS: Feedback and non-feedback systems, Effects of feedback on sensitivity (to parameter variations), stability, overall gain etc.

UNIT-II:
TIME RESPONSE ANALYSIS: Standard test signals, time response of first order and second order systems, steady-state errors and error constants, design specification of second-order-systems.
STABILITY:The concept of stability ,necessary conditions for stability, Hurwitz stability criterion, Routh stability criterion, Relative stability analysis.
THE ROOT LOCUS TECHNIQUE:The Root locus concept, construction /development of root loci for various systems, stability considerations.

UNIT-III:
FREQUENCY RESPONSE & STABILITY ANALYSIS: Correlation between time and frequency response, Polar Plots, Nyquist plots, Bode Plots, Nyquist stability criterion, Gain margin & Phase margin, relative stability using Nyquist Criterion, frequency response specifications.

UNIT-IV:
COMPENSATION OF CONTROL SYSTEMS: Necessity of compensation, Phase lag compensation, phase lead compensation , phase lag lead compensation, feedback compensation .
STATE VARIABLE ANALYSIS : Concept of state,state variable and state model, state models for linear continuous time systems, diagonalization solution of state equations, concept of controllability and observability.

NOTE :

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

TEXT BOOK:

1. Control System Engg : I.J.Nagrath & M.Gopal; New Age India.

Reference Books:

1. Automatic Control Systems : B.C.Kuo; PHI.
2. Modern Control Engg : K.Ogata; PHI.
3. Control Systems: Principles & Designing : Madan Gopal; TMH.

B.TECH V1th SEMESTER
VHDL AND DIGITAL DESIGN
(ECE-304E)

L	T	P		
3	1	-	Theory :	100
			Sessional :	50
			Time :	3Hrs

UNIT I:

INTRODUCTION: History. Why use VHDL ? Hardware design construction, design levels, HDLs Hardware simulation and synthesis. Using VHDL for design synthesis, terminology.

PROGRAMMABLE LOGIC DEVICES :Why use programmable logic ? What is a programmable logic device ? Block diagram, macrocell structures and characteristics of PLDs and CPLDs. Architecture and features of FPGAs. Future direction of programmable logic.

UNIT II:

BEHAVIORAL MODELING:Entity declaration, architecture body, process statement, variable assignment, signal assignment. Wait, If, Case, Null, Loop, Exit, Next and Assertion statements. Inertial and transport delays, Simulation deltas, Signal drivers.

DATA FLOW AND STRUCTURAL MODELLING:Concurrent signal assignment, sequential signal assignment, Multiple drivers, conditional signal assignment, selected signal assignment, block statements, concurrent assertion statement, component declaration, component instantiation.

UNIT III:

GENERICS AND CONFIGURATIONS :Genericcs, Why configurations ?, default configurations, component configurations. Genericcs in configuration. Generic value specification in architecture, block configurations, architecture configurations.

SUBPROGRAMS AND PACKAGES :Subprograms – functions, procedures, declarations. Package declarations, package body, use clause, predefinal package standard. Design libraries, design file.

UNIT IV:

ADVANCED TOPICS :Generate Statements, Aliases, Qualified expressions, Type conversions, Guarded signals, User defined attributes, Predefined attributes., VHDL synthesis.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. D. Perry , VHDL, 3rd Ed.- TMH.
2. J.Bhasker, A.VHDL- Primer, PHI.
3. Skahil, VHDL for Programmable logic- 2nd Ed – Wiley.

B.TECH V1 SEMESTER
DIGITAL SIGNAL PROCESSING
(ECE- 306E)

L	T	P
3	2	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT – I:
DISCRETE TRANSFORMS: Z- transform and its properties, Inversion of Z-transform, One sided Z-transform and solution of differential equations. Analysis of LTI systems in Z-domain, causality, stability, schur-cohn stability test; relationship between Z-transform and Fourier transform. Frequency selective filters; all pass filters, minimum-phase, maximum-phase and mixed-phase systems.
Frequency domain sampling and DFT; properties of DFT, Linear filtering using DFT, Frequency analysis of signals using DFT, radix 2, radix-4, goertzel algorithm, Chirp Z-transform, applications of FFT algorithm, computation of DFT of real sequences. Quantization effects in computation of DFT.

UNIT – II:
IMPLEMENTATION OF DISCRETE TIME SYSTEMS: Direct form, cascade form, frequency sampling and lattice structures for FIR systems. Direct forms, transposed form, cascade form parallel form. Lattice and lattice ladder structures for IIR systems. State space structures Quantization of filter co-efficient structures for all pass filters.

UNIT – III:
DESIGN OF FIR FILTERS: Characteristics of practical frequency selective filters. Filters design specifications peak pass band ripple, minimum stop band attenuation. Four types of FIR filters Design of FIR filters using windows. Kaiser window method comparison of design methods for FIR filters Gibbs phenomenon, design of FIR filters by frequency sampling method, design of optimum equiripple FIR filters, alternation theorem.

UNIT – IV:
DESIGN OF IIR FILTERS: Design of IIR filters from analog filters, Design by approximation of derivatives, Impulse invariance method bilinear transformation method characteristics of Butterworth, Chebyshev, and Elliptical analog filters and design of IIR filters, Frequency transformation, least square methods, design of IIR filters in frequency domain.

NOTE:
The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. John G. Proakis, Digital Signal Processing, PHI
2. S. K. Mitra, Digital Signal Processing , TMH
3. Rabiner and Gold, Digital Signal Processing, PHI
4. Salivahan, Digital Signal Processing , TMH
5. Digital Signal Processing: Alon V. Oppenhelm;PHI

B. TECH. VI SEMESTER
DIGITAL COMMUNICATION
(ECE-308E)

L	T	P
3	1	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT – I:
PULSE MODULATION: sampling process, PAM and TDM; aperture effect. PPM noise in PPM, channel Bandwidth, Recovery of PAM and PPM signals Quantization process, quantization noise, PCM, μ Law and A- law compressors. Encoding, Noise in PCM, DM, delta sigma modulator, DPCM, ADM.

UNIT – II:
BASE BAND PULSE TRANSMISSION: Matched filter and its properties average probability of symbol error in binary enclosed PCM receiver, Intersymbol interference, Nyquist criterion for distortionless base band binary transmission, ideal Nyquist channel raised cosine spectrum, correlative level coding Duo binary signalling, tapped delay line equalization, adaptive equalization, LMS algorithm, Eye pattern.

UNIT – III:
DIGITAL PASS BAND TRANSMISSION: Pass band transmission model; gram Schmidt orthogonalization procedure, geometric Interpretation of signals, Response of bank of correlaters to noise input, detection of known signal in noise, Hierarchy of digital modulation techniques, BPSK, DPSK, DEPSK, QPSK, systems; ASK, FSK, QASK, Many FSK, MSK, Many QAM, Signal space diagram and spectra of the above systems, effect of intersymbol interference, bit symbol error probabilities, synchronization.

UNIT – IV:
SPREAD SPECTRUM MODULATION: Pseudonoise sequence, A notion of spread spectrum, direct sequence spread spectrum with coherent BPSK, signal space dimensionality & processing gain, probability of error, frequency spread spectrum, CDM.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

Suggested Books:

1. John G. Proakis, Digital Communication, PHI
2. Taub & Schilling, Principles of Communication, TMH
3. Simon Haykin, Communication systems, John Wiley & Sons

B.TECH V1 SEMESTER
COMPUTER COMMUNICATION NETWORKS
(ECE-310E)

L	T	P
3	1	-

Theory	:	100
Sessional	:	50
Time	:	3Hrs

UNIT – I:
INTRODUCTION: Uses of Computer Networks, Network Hardware, Network Software, Reference models, Examples of Networks & Data communication Services, Network Standardization.
THE PHYSICAL LAYER: The Theoretical basis for Data communication, Transmission media, Wireless Communication, The Telephone System, Narrowband ISDN, Broadband ISDN and ATM, Cellular Radio, Communication Satellites.

UNIT – II:
THE DATA LINK LAYER: Data Link Layer Design issues, Error Detection & correction, Elementary Data Link protocols, Sliding Window Protocols, Protocol Specification & Verification, Example of Data Link Protocols.
THE MEDIUM ACCESS SUBLAYER: Aloha Protocols, LAN Protocols, IEEE Standards, Fiber optic Networks, Satellite Networks, Packet switching, radio Networks.

UNIT – III:
NETWORK LAYER: Design issues, routing algorithms, congestion control Algorithms, internetworking.
TRANSPORT & SESSION LAYER: Protocol design issues, connection Management, remote procedure calls.

UNIT – IV:
PRESENTATION LAYER: Design issues, abstract Syntax notation, data compression technique, cryptograph.
APPLICATION LAYER: Design issues, file transfer, access and management, electronic mail, virtual terminals, applications and examples.

Suggested Books:

1. Tanenbaum A.S, Computer Networks, PHI.
2. Forouzan B.A, Data Communications and Networking, Tata-Mc-Graw Hill.
3. Stallings W, Data and Computer Communications, PHI.
4. Ahuja V, Design and Analysis of Computer Communication, McGraw Hill.
5. Bee K.C.S, Local Area Networks, NCC Pub.
6. Davies D. W. Barber, Computer Networks and their Protocols, John Wiley.

NOTE:

The question paper shall have eight questions in all organized into four sections, each section having two questions from each of the four units. The candidate shall have to attempt five questions in all , selecting at least one question from each unit.

B.TECH VI SEMESTER
DIGITAL COMMUNICATION PRACTICAL
(ECE-312E)

L	T	P
-	-	3

Sessional	:	50
Viva	:	25
Time	:	3Hrs

LIST OF EXPERIMENTS:

1. To Study PSK
2. To Study FSK
3. To Study IF Amplifier
4. To Study Balanced Modulator & Demodulator
5. To Study PCM
6. Setting up a Fiber Optic Analog Link
7. Setting up a Fiber Optic Digital Link
8. Losses in Optical Fiber
9. Measurement of Numerical Aperture
10. Time Division multiplexing of signals.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope

B.TECH V1th SEMESTER
ELECTRONICS DESIGN PRACTICAL
(ECE-314E)

L	T	P
-	-	3

Exam	:	25
Sessional	:	50
Time	:	3Hrs

LIST OF EXPERIMENTS:

1. Design a single stage R C Coupled amplifier and plot its gain frequency response.
2. Design a two stage R C Coupled amplifier and plot its gain frequency response.
3. Design a R C Phase shift oscillator using IC 741.
4. Design a wein bridge oscillator.
5. Design a square wave generator using IC 555.
6. Design a 4 : 1 multiplexer and 1 : 4 demultiplexer using logic gates.
7. Design a parallel parity bit generator using ICs.
8. Design a digital to analog converter using ICs.
9. Design a digital frequency meter (0-999HZ) using IC 555 for monoshot, IC-7404,7408,7490,7447.
10. Design a controller such that LEDs glow in pairs sequentially using IC 7490 and LEDs.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope

B.TECH V1th SEMESTER
VHDL PRACTICAL
(ECE-316E)

L	T	P			
-	-	3	Exam	:	50
			Sessional	:	50
			Time	:	3Hrs

LIST OF EXPERIMENTS:

1. Write a VHDL Program to implement a 3 :8 decoder.
2. Write a VHDL Program to implement a 8:1 multiplexer using behavioral modeling.
3. Write a VHDL Program to implement a 1 :8 demultiplexer using behavioral modeling.
4. Write a VHDL Program to implement 4 bit addition/subtraction.
5. Write a VHDL Program to implement 4 bit comparator.
6. Write a VHDL Program to generate Mod- 10 up counter.
7. Write a VHDL Program to generate the 1010 sequence detector. The overlapping patterns are allowed.
8. Write a program to perform serial to parallel transfer of 4 bit binary number.
9. Write a program to perform parallel to serial transfer of 4 bit binary number.
10. Write a program to design a 2 bit ALU containing 4 arithmetic & 4 logic operations.

NOTE: At least 10 experiments are to be performed with atleast 7 from above list, remaining 3 may either be performed from the above list or designed & set by concerned institution as per the scope